REMARKS

In the Office Action dated February 5, 2004, claims 1-24 were pending. Claims 13-24 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al. Portions of the drawings and specification are objected.

In this response, claims 15-16 have been canceled without prejudice. Claims 1-2, 4-9, 13-14, and 17-21 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicant regards as his invention. Thus, claims 1-14 and 17-24 remain pending. No new matter has been added. In addition, portions of the specification have been amended. Reconsideration of this application as amended is respectfully requested.

Portions of the drawings were objected because the drawings must show every feature of the invention specified in the claims. In view of the foregoing claim amendments, it is respectfully submitted that the objections have been overcome.

Portions of the specifications were objected. In view of the foregoing specification amendments, it is respectfully submitted that the objections have been overcome.

Portions of the claims were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In view of the foregoing amendments, it is respectfully submitted that the rejections have been overcome.

With respect to the double patenting rejections, it is respectfully submitted that terminal disclaimers will be submitted when the present application in condition of allowance.

Claims 1-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al. Applicant submits the present invention as claimed includes limitations not disclosed or taught by the cited references. Specifically, independent claim 1 recites:

1. A method comprising:

enabling a special programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for internal program verification and wherein enabling special programming mode disables the internal program verification by the automation circuitry of the memory;

programming a plurality of words into the memory during the special programming mode without having the automation circuitry of the memory to perform the internal program verification; and

exiting the special programming mode of the memory after the plurality of words have been programmed into the memory.

(Emphasis added)

Independent claim 1 includes limitations that enabling a special programming mode would disable the internal program verification performed by the memory. During the special programming mode, multiple words can be programmed into the memory without having the memory to perform the internal program verification. The above limitations are absent from the cited references, individually or in combination.

As acknowledged by the Examiner, Application Note AP-629 or AP-678 fails to disclose the limitation that entering into the special programming mode would disables the internal program verification (Office Action, page 11). However, the Examiner maintains that Olivo discloses such limitations. Specifically, the Examiner stated:

> "Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines and 7-12 32-36, e.g.)."

(Office Action, page 11, emphasis added)

Applicant respectfully disagrees. It is respectfully submitted that the test circuitry of Olivo disables the internal state machine, instead of internal program verification of the memory, during the testing (see, col. 2, lines 9-37 of Olivo). It is respectfully submitted that disabling an internal state machine is not the same as disabling internal program verification. There is no mention of disabling internal program verification within the cited section of Olivo as suggested by the Examiner.

In addition, disabling the internal state machine of Olivo is not related to program verification. Rather, by disabling the internal state machine, the addresses occupied by the internal state machine can be used for other purposes, such as testing. Specifically, Olivo stated:

> "Consequently, having excluding the internal state machine 11, the addresses can be used freely and, using the above listed control signals with their new meaning, the desired cells can be programmed and their correctness can be verified."

(Olivo col. 4, lines 32-36, emphasis added).

Thus, Olivo fails to disclose or suggest disabling internal program verification. Olivo further states:

> "Verification is performed by a comparison of the values present after memory programming with the correct ones supplied through the data bus 3. The signal CEN also returns to a low logic value Vil and the circuit is ready to perform a new test or return to normal operation.
>
> The test method in accordance with the present invention has the following advantages: The memory matrix test can be performed in a manner fully independent of control unit operation. The duration of the programming pulse and that of the verification phase are not bound to the internal time base and can thus be selected at will. The sequence of performance of the actual test is compatible with that used for testing EPROM memories of the known art and thus permits use of the same circuitry equipment for its performance."

(Olivo col. 4, line 63 to col. 5, line 10, emphasis added).

Clearly, these verification operations are performed within the memory (e.g., internal program verification), rather than by an external host processor as claimed in the present invention. Again, there is no mention of disabling internal program verification within the cited section of Olivo as suggested by the Examiner. Such a suggestion can only be found in Applicant's own disclosure. It would be impermissible hindsight to use Applicant's own disclosure to against the Applicant.

Furthermore, there is no suggestion within the cited references to combine with each other. Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claim 13 includes limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, it is respectfully submitted that independent claim 13 is patentable over the cited references.

The rest of the claims depend from one of the above independent claims, thus include all of the distinct features of the respective independent claim, and therefore, for the reasons similar to those discussed above, are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,
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